CLAIMS

I Claim:

1. A semiconductor integrated circuit, comprising:

a plurality of circuit blocks capable of transitions from an operating state to a standby state and from a standby state to an operating state; and,

a control circuit which controls, in event-driven fashion, the back-gate voltages of transistors forming logic elements of said circuit blocks, based on a finite state machine that stipulates in advance each of the state transitions of said plurality of circuit blocks.

2. The semiconductor integrated circuit according to Claim 1, wherein said control circuit controls said back-gate voltages such that, when said circuit blocks are in the standby state, the threshold voltages of said transistors are increased.

3. The semiconductor integrated circuit according to Claim 1, wherein said control circuit controls said back-gate voltages such that, when said circuit blocks are in the operating state, the threshold voltages of said transistors are decreased.

4. The semiconductor integrated circuit according to Claim 1, further comprising:

a common power supply line to supply power to each of said plurality of circuit blocks;

a common ground line to ground each of said plurality of circuit blocks; and

switching elements to perform electrical connection/disconnection between said circuit blocks and at

least either one of said common power supply line and said common ground line,

wherein said control circuit controls the connection/disconnection of said switching elements in an event-driven fashion, based on said finite state machine.

5. A semiconductor integrated circuit, comprising:

a plurality of circuit blocks capable of transitions from an operating state to a standby state and from a standby state to an operating state;

channels to actively issue operation requests or to passively receive operation requests, through communications between said circuit blocks by a CSP method; and,

ports connecting circuit blocks to each other via said channels;

wherein said channels and ports control the back-gate voltages of transistors constituting logic elements of said circuit blocks, according to the operating states of said circuit blocks.

6. The semiconductor integrated circuit according to Claim 5, wherein said channels and ports control said back-gate voltages such that, when said circuit blocks are in the standby state, the threshold voltages of said transistors are increased.

7. The semiconductor integrated circuit according to Claim 5, wherein said channels and ports control said back-gate voltages such that, when said circuit blocks are in the operating state, the threshold voltages of said transistors are decreased.

8. The semiconductor integrated circuit according to Claim 5, further comprising:

a common power supply line to supply power to each of said plurality of circuit blocks;

a common ground line to ground each of said plurality of circuit blocks; and

switching elements to perform electrical connection/disconnection between said circuit blocks and at least either one of said common power supply line and said common ground line,

wherein said channels and ports control the connection/disconnection of said switching elements according to the operating states of said circuit blocks.

9. The semiconductor integrated circuit according to Claim 1, wherein said transistors are double-gate TFTs.

10. The semiconductor integrated circuit according to Claim 9, wherein said double-gate TFTs has the drain and source extensions of LDD structure.

11. The semiconductor integrated circuit according to Claim 9, wherein, in said double-gate TFTs, the gate electrode and back-gate electrode are positioned in opposition with the channel region therebetween, and are formed in substantially the same shape such that the shapes thereof projected onto said channel region overlap.

12. The semiconductor integrated circuit according to Claim 10, wherein said back-gate electrode is formed such that the shape projected onto the channel region overlaps wholly or partially with said LDD region.

13. Electronic equipment comprising a semiconductor integrated circuit according to any of the Claims 1 through 12.

14. A back-gate voltage control method, wherein the back-gate voltages of transistors forming logic elements of a plurality of circuit blocks capable of transitions from an operating state to a standby state and from a standby state to an operating state are controlled based on a finite state machine which stipulates in advance each of the state transitions of said plurality of circuit blocks.

15. The back-gate voltage control method according to Claim 14, wherein said back-gate voltages are controlled such that, when said circuit blocks are in the standby state, the threshold voltages of said transistors are increased.

16. The back-gate voltage control method according to Claim 14, wherein said back-gate voltages are controlled such that, when said circuit blocks are in the operating state, the threshold voltages of said transistors are decreased.

17. A back-gate voltage control method, to control back-gate voltages in a semiconductor integrated circuit comprising a plurality of circuit blocks capable of transitions from an operating state to a standby state and from a standby state to an operating state, channels to actively issue operation requests or to passively receive operation requests through communications between said circuit blocks by a CSP method, and ports connecting circuit blocks to each other via said channels,

wherein said channels and ports control the back-gate voltages of transistors constituting logic elements of said

circuit blocks, according to the operating states of said circuit blocks.

18. The back-gate voltage control method according to Claim 17, wherein said back-gate voltages are controlled such that, when said circuit blocks are in the standby state, the threshold voltages of said transistors are increased.

19. The back-gate voltage control method according to Claim 17, wherein said back-gate voltages are controlled such that, when said circuit blocks are in the operating state, the threshold voltages of said transistors are decreased.